

CLAIMS

What is claimed is:

- 5 1. A stacked pad for processing substrates for the fabrication of electronic devices, the stacked pad comprising a top pad having a Shore D hardness greater than or equal to about 40 and a subpad having a Shore D hardness substantially equal to the hardness of the top pad.
- 10 2. The stacked pad of claim 1, wherein the top pad has a Shore D hardness from about 40 to about 70 and all ranges and values subsumed therein.
3. The stacked pad of claim 1, wherein the top pad has a Shore D hardness from about 50 to about 60 and all ranges and values subsumed therein.
- 15 4. A stacked pad for processing substrates for the fabrication of electronic devices, the stacked pad comprising a top pad having a Shore D hardness from about 40 to about 70, a subpad having a Shore D hardness equal to the hardness of the top pad, and an adhesive sandwiched between the top pad and the subpad to bind the top pad
- 20 to the subpad.
5. A method of chemical mechanical polishing, the method comprising the steps of:
- 25 A. providing a substrate having a surface for fabricating electronic devices, the surface comprising a dielectric material having a dielectric constant less than two;
- B. providing a stacked pad, the stacked pad comprising a top pad having a Shore D hardness from about 40 to about 70 and a subpad having a Shore D hardness substantially equal to the hardness of the top pad; and
- 30 C. contacting the top pad with the surface and planarizing the surface with the stacked pad.
6. The method of claim 5 further comprising the step of conditioning the top pad using a down force less than about 0.24 psi (1.7 KPa).

7. The method of claim 5 further comprising the step of conditioning the top pad after planarization of a plurality of the substrates and performing the conditioning using a down force less than about 0.24 psi (1.7 KPa).

5 8. The method of claim 5 further comprising the step of planarization of five of the substrates before conditioning the top pad and performing the conditioning using a down force less than about 0.24 psi (1.7 KPa).

10 9. The method of claim 5 further comprising the step of repeating step A through step C a plurality of times before conditioning the top pad.

10. The method of claim 5 further comprising the step of repeating step A through step C a plurality of times before conditioning the top pad using a down force less than about 0.24 psi (1.7 KPa).

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11. The method of claim 5 further comprising conditioning the top pad only prior to the first planarization and using the stacked pad for planarizing a multiplicity of the substrates.

20 12. The method of claim 5 further comprising processing a plurality of wafers between pad conditionings.

13. The method of claim 5, wherein the stacked pad is conditioned before the first planarization.

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14. The method of claim 5, wherein the stacked pad is conditioned on a tool other than a polishing tool before the first planarization.

15. A method of chemical mechanical polishing, the method comprising the steps of:

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- A. providing a substrate having a surface for fabricating electronic devices;
- B. providing a stacked pad, the stacked pad comprising a top pad and a subpad, wherein the hardness or modulus of the top pad substantially equals the hardness or modulus of the subpad; and

C. contacting the top pad with the surface and planarizing the surface with the stacked pad.

5 16. The method of claim 15, wherein the top pad and subpad have a compressibility of about 1.8%.

17. The method of claim 15, wherein the top pad and subpad have a substantially equal density and the density is in the range from about 0.5 to about 0.7 grams/cc.

10 18. The method of claim 15, wherein the top pad and subpad have a substantially equal pore size range and the pore size range is in the range from about 0.5 to about 0.7 grams/cc.

15 19. The method of claim 15, wherein the top pad and subpad have a substantially equal density and the density is in the range from about 0.5 to about 0.7 grams/cc and the top pad and sub pad have substantially equal hardness and the Shore D hardness is greater than about 47.

20 20. A stacked pad for processing substrates for the fabrication of electronic devices, the stacked pad comprising a polyurethane impregnated felt top pad having Shore D hardness from about 51 to about 54, a polyurethane impregnated felt subpad having Shore D hardness equal to the hardness of the top pad, and an adhesive sandwiched between the top pad and the subpad to bind the top pad to the subpad; the top pad and the subpad having density of 0.58 +/- 0.04, a fiber to polymer resin ratio of 55:45,
25 a felt density of 0.32 grams/cc, and a compressibility of 1.8%, wherein the properties of the top pad are substantially uniform and the properties of the sub pad are substantially uniform.